## UNITED STATES DISTRICT COURT DISTRICT OF MASSACHUSETTS

SINGULAR COMPUTING LLC,	Civil Action No. 1:19-cv-12551-FDS	
Plaintiff,	Hon. F. Dennis Saylor IV	
V.	Tron. 1 · Beimie euglei 1 ·	
GOOGLE LLC,		
Defendant.		

# STATEMENT OF UNDISPUTED MATERIAL FACTS IN SUPPORT OF PLAINTIFF'S MOTION FOR PARTIAL SUMMARY JUDGMENT OF NO INVALIDITY UNDER 35 U.S.C. § 101

Pursuant to Fed. R. Civ. P. 56 and Local Rule 56-2, plaintiff, Singular Computing LLC ("Singular"), submits the following Statement of Undisputed Material Facts in support of its motion for partial summary judgment of no invalidity under 35 U.S.C. § 101.

No.	Statement of Fact	Supporting Evidence
1.	Singular is the owner, by assignment of U.S. Patent No. 8,407,273 ("the '273 patent").	Amended Complaint, ¶¶ 27-28; U.S. Patent No. 8,407,273 (Dkt. No. 112-2).
2.	Singular is the owner, by assignment of U.S. Patent No. 9,218,156 ("the '156 patent").	Amended Complaint, ¶¶ 27-28; U.S. Patent No. 9,218,156 (Dkt. No. 112-3).
3.	On March 31, 2021, the Court issued an memorandum and Order denying Defendant's Motion to Dismiss.	Dkt. No. 51.
4.	On July 27, 2022, the Court issued a Memorandum and Order on Claim Construction.	Dkt. No. 354.
5.	Claim 53 of the '273 patent recites the following:  A device:	'273 patent.
	comprising at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on	

No.	Statement of Fact	Supporting Evidence
	a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	
	wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;	
	wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	
6.	Claim 7 of the '156 patent recites the following:	'156 patent.
	A device comprising:  at least one first low precision high- dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	
	wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each	

No.	Statement of Fact	Supporting Evidence
	specific input from the at least X % of the	
	possible valid inputs to the first operation,	
	of the numerical values represented by the	
	first output signal of the LPHDR unit	
	executing the first operation on that input	
	differs by at least Y=0.05% from the result of an exact mathematical calculation of the	
	first operation on the numerical values of	
	that same input;	
	that same input,	
	at least one first computing device adapted	
	to control the operation of the at least one	
	first LPHDR execution unit;	
	wherein the at least one first computing	
	device comprises at least one of a central	
	processing unit (CPU, a graphics	
	processing unit (GPU), a field	
	programmable gate array (FPGA), a microcode-based processor, a hardware	
	sequencer, and a state machine; and,	
	sequencer, and a state macrime, and,	
	wherein the number of LPHDR execution	
	units in the device exceeds by at least one	
	hundred the non-negative integer number	
	of execution units in the device adapted to	
	execute at least the operation of	
	multiplication on floating point numbers	
	that are at least 32 bits wide.	

Dated: April 28, 2023 Respectfully submitted,

#### /s/ Paul J. Hayes

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ATTORNEYS FOR THE PLAINTIFF

#### **CERTIFICATE OF SERVICE**

I certify that on April 28, 2023, all counsel of record who have consented to electronic service are being served with a copy of this documents via the Court's CM/ECF system.

/s/ Paul J. Hayes